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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,499	01/22/2002	Jin-Yuan Lee	JCLA8534	7456

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EXAMINER	
THAI, LUAN C	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,499	LEE ET AL.	
	Examiner	Art Unit	
	Luan Thai	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *61-63,70-81 and 83-89* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *61-63,70-81 and 83-89* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the amendment filed August 03, 2004.

Claims **61-63, 70-81, and 83-89** are pending in this application.

Claims **90-93 and 95-100** have been cancelled.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 61-62, 72, 74, 78, 81, 83, 84 and 89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al (5,049,980 of record) in view of Eichelberger et al (6,396,148 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 61-62, 72, 74, 78, 81, 83, 84 and 89, Saito et al (see specifically figures 1-5) disclose a chip packaging method comprising: providing an organic (e.g., thermosetting plastic) substrate (1) with a surface; providing a plurality of dies (2), wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads (3) located on the active surface, whereas the backside of each die is adhered to the surface of the organic substrate; forming a first dielectric layer (4) on top of the surface of the substrate (1) and the active surface of the dies (2), and

patterning the first dielectric layer (4) to form a plurality of first thru-holes (5) (see figure 2); filling the thru-holes (5) with a conductive material to form a plurality of first vias (6), forming a first patterned wiring layer comprising a plurality of patterned lines (7) on top of the first dielectric layer (4) and over the active surface of the dies (2), wherein the first patterned wiring layer of copper (7) is electrically connected to the metal pads (3) of the dies (2) through the first dielectric layer (4) by the vias (6) and extends to a region outside of an area above the active surfaces of the dies; allocating a second dielectric layer (9) on top the first dielectric layer and the first patterned wiring layer; allocating a second patterned wiring layer (11) on top the second dielectric layer (9), wherein the second patterned wiring layer is electrically connected to the first patterned wiring layer (7) at bonding pads via conductive vias or bonding points (10) formed through the second dielectric layer (9). Saito does not implicitly teach a singularizing step being applied for forming multiple chip package structures.

Eichelberger et al while related to a similar method of forming a semiconductor package teach the method steps of processing a plurality of chips or dies on a single panel and then sawing the panel into individual package modules (Col. 8, lines 46-56). It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that combining the Eichelberger et al's teachings with Saito et al's invention would have been beneficial because forming plurality of chip or dies on a single panel and then performing the sawing step, as taught by Eichelberger et al, helps Saito's invention to improve the production quantity and reduce the production cost.

3. Claims 76-77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al (5,049,980 of record) and Eichelberger et al (6,396,148 of record), as applied to claim 61 above, and further in view of Choi (6,428,377).

Regarding claims 76-77, the proposed method of Saito et al. and Eichelberger et al. discloses all the method steps of the claimed invention as detailed above with the exception of specifying the process of forming the patterned lines (e.g., "electroplating").

"Electroplating" technique, however, is one of well-known metal-depositing techniques in semiconductor art, as disclosed by Choi (Col. 7, lines 5-17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the electroplating technique to form the metal patterned lines in the proposed method of Wachtler et al. and Eichelberger et al., since such metal depositing technique is well known in the art, as taught by Choi, and the applying of such technique is held to be within the ordinary designing ability expected of a person skilled in the art.

4. Claims 61-63, 72-75, 78-81, and 83-89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wachtler et al (6,274,391 of record) in view of Eichelberger et al (6,396,148 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 61-63, 72-75, 78-81, and 83-89, Wachtler et al (see specifically figures 8-22) disclose a chip packaging method comprising: providing an organic substrate (12) made of molded plastic (e.g., being considered as the claimed of "polymer resin", "epoxy resin" or "imide resin"); providing a plurality of dies (16)/(52) (Col. 11,

lines 41-67 and Col. 12, lines 1-9), which are performed same functions or different functions (Col. 7, lines 58+), wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads (Col. 8, lines 63-67) located on the active surface, whereas the backside of each die is adhered to the surface of the organic substrate by a adhesive (Col. 8, lines 53+); forming a first dielectric layer (26/24) of polyimide on top of the surface of the substrate (12) and over the active surface of the dies (Col. 8, lines 59+); patterning the first dielectric layer (26/24) to form a plurality of first thru-holes (28) (see figures 11-12); forming a first plurality of patterned lines (34/36) on top of the first dielectric layer (24/26), wherein the first patterned lines fills the first thru-holes (28) and electrically connected to the metal pads of the dies (16). Wachtler et al further disclose the step of forming a second dielectric layer (36/38) on top of the first patterned lines (32/34); forming a plurality of second thru-holes (40) through the second dielectric layer (see figures 16-17); forming a second patterned lines (42) on top the second dielectric layer (36/38), wherein the second patterned lines extend through the second dielectric layer, are electrically connected to the first patterned lines, and has a plurality of second bonding pads (44); forming a patterned passivation layer (46) on top of the second patterned lines and exposing the second bonding pads (44); attaching solder balls (22) to the bonding pads (44). Wachtler does not implicitly teach the method step of singularizing to form multiple chip package structures.

Eichelberger et al while related to a similar method of forming a semiconductor package teach the method steps of processing a plurality of chips or dies on a single panel and then sawing the panel into individual package modules (Col. 8, lines 46-56). It would

have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that combining the Eichelberger et al's teachings with Wachtler's invention would have been beneficial because forming plurality of chip or dies on a single panel and then performing the sawing step, as taught by Eichelberger et al, helps Wachtler's invention to improve the production quantity and reduce the production cost.

Note that plastic is considered: as "polyimide resin" (see U.S. Pat. No. 3,677,112 (column 3, line 3) to Keniston), as "epoxy resin" (see U.S. Pat. No. 5,606,198, column 1, line 23, to Ono et al., US. Pat. No. 6,242,987, column 4, lines 20-21, to Schopf et al., and US. Pat. No. 5,939,214, column 2, lines 23-24, to Mahulikar et al.), as "imide resin" (see US. Pat. No. 4,235,498, column 5, line 7, to Snyder).

5. Claims 76-77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wachtler et al (6,274,391 of record) and Eichelberger et al (6,396,148 of record), as applied to claim 61 above, and further in view of Choi (6,428,377).

Regarding claims 76-77, the proposed method of Wachtler et al. and Eichelberger et al. discloses all the method steps of the claimed invention as detailed above except for specifying the process of forming the patterned lines (e.g., "electroplating"). "Electroplating" technique, however, is one of a plurality of well-known metal depositing techniques in semiconductor art, as disclosed by Choi (Col. 7, lines 5-17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the electroplating technique to form the metal pattern lines in the proposed method of Wachtler et al. and Eichelberger et al., since such metal depositing technique is well

known in the art, as taught by Choi and the applying of such technique is held to be within the ordinary designing ability expected of a person skilled in the art.

6. Claims 61-62, 70-81, and 83-89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al (6,396,148 of record) in view of Marcinkiewicz (6,025,995).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 61-62, 70-81, and 83-89, Eichelberger et al (see specifically figures 1-7) disclose a chip packaging method comprising: providing a substrate (101) with a surface; providing a plurality of dies (102), wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads (107) located on the active surface, whereas the backside of each die is adhered to the surface of the substrate by a adhesive (103); forming a filling layer (104) of polymer or epoxy over the substrate (101) and surrounding the peripheral of the dies (102), wherein a top surface of the filling layer (104) being planar to the active surface of the dies (104) (see figures 3A and 4A); forming a first dielectric layer (106) of polyimide over the top surface of the substrate (101) and over the active surface of the dies (102), and patterning the first dielectric layer (106) to form a plurality of first thru-holes (122) (see figures 3D and 4B); forming a plurality of first patterned lines (108) by electro-plating, wherein the first patterned lines (108) is electrically connected to the metal pads (107) of the dies (102) through the first dielectric layer (106), and wherein the first patterned lines (108) has a plurality of first bonding pads electrically connected to solder balls (110). Eichelberger et al further disclose: the method step of forming a patterned passivation

layer (109) (or 232) on top of the first dielectric patterned lines (108) (or 206) and exposing the first bonding pads on the first patterned wiring layer (108) for solder balls (110) electrically connected to, as disclosed in figure 1. Eichelberger et al further disclose a step of singularizing the chip package structure to form a single chip package (Col. 8, lines 46+), and that the similar steps as described above can be repeated until all required patterned lines and dielectric layer have been completed (Col. 8, lines 53+). (Noted that figures 6C-7C also disclose passivation layer "232" is formed on top of the first dielectric patterned wiring layer "206" and exposing the first bonding pads on the first patterned wiring layer "209" for solder balls "234" electrically connected to. Eichelberger et al., however, do not explicitly teach the substrate comprising organic (claim 61) such as: plastic (claim 80), thermal plastic (claim 81), polymer resin (claim 86), epoxy resin (claim 87), or imide resin (claim 88).

Marcinkewicz while related to a similar semiconductor structure design teaches the substrate (14) in the integrated circuit module (10) could be made by different kinds materials such as: ceramic, plastic, silicon or any III-V of similar compound, etc., (Col. 3, lines 58+), which are considered as known materials for forming a substrate in semiconductor art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a known material, such as plastic or silicon (organic material), to form the substrate in Eichelberger et al.'s chip package, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. Note that plastic (organic material) is considered: as "polyimide resin" (see U.S. Pat. No. 3,677,112

(column 3, line 3) to Keniston), as "epoxy resin" (see U.S. Pat. No. 5,606,198, column 1, line 23, to Ono et al., US. Pat. No. 6,242,987, column 4, lines 20-21, to Schopf et al., and US. Pat. No. 5,939,214, column 2, lines 23-24, to Mahulikar et al.), as "imide resin" (see US. Pat. No. 4,235,498, column 5, line 7, to Snyder).

7. Claim 63 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al (6,396,148, called "Eic-148" of record) and Marcinkiewicz (6,025,995), as applied to claim 61 above, and further in view of Eichelberger et al (5,841,193, called "Eic-193" of record).

Regarding claim 63, the proposed method of Eic-148 and Marcinkiewicz discloses all the limitations of the claimed invention as detailed above except for not explicitly teaching the dies performing different functions.

Eic-193 while related to a similar chip packaging method teaches that the product formed by such method can comprise different dies (Col. 8, lines 55+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the proposed method of Eic-148 and Marcinkiewicz with the dies performing different functions, since such application is commonly used in the art, as taught by Eic-193, and it is held to be within the ordinary designing ability expected of a person skilled in the art.

Conclusion

8. Applicant's arguments with respect to claims **61-63, 70-81, and 83-89** have been fully considered, but they are deemed to be moot in view of the new grounds of rejection.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action because the changes (e.g., the underlined portions) in claims 61, 70, 72-81 and 83-

89 raise new issues that would require further consideration and/or search. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:45 AM - 4:15 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Luan Thai
Primary Examiner
Art Unit 2829
October 14, 2004